# Substrate Noise Coupling in Mixed-signal Integrated Circuits*

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**Abstract** In this paper, the substrate noise coupling in the mixed-signal ICs and its effect on the analog/digital circuits are investigated. The heavily doped substrate with an epitaxial layer is adopted. Two benchmark circuits are evaluated. Proper simulation technique for the mixed-signal circuits in SPICE for high speed and high frequency operations is developed.

**Key words** substrate noise; coupling; mixed-signal IC; model

With the rapid development of wireless communication circuits, the substrate noise becomes a major concern in the design of mixed-signal ICs due to the increasing chip complexity for RF applications. In mixed-signal ICs, both analog and digital circuits are fabricated on the same substrate. In the digital portion, a large number of gates undergo transition periodically at high frequency. When such transition occurs, a spike of current is absorbed from the power bus. Usually a great portion of this current passes through the ground bus through direct feed through or it is injected into the substrate. The chip complexity and higher level of integration usually do not allow the analog and digital grounds to tie together. The cumulative contribution of currents injected by switching gates in the substrate is felt in the sensitive analog portion circuits in form of spurious signal, which is known as substrate noise. This high-speed substrate noise changes the desired analog output and degrades the overall IC performance.

One of the most important issues in mixed-signal design is to model the substrate and to predict the signal coupling between the digital circuits and the analog circuits on the same substrate correctly. The design methodology to reduce the substrate noise coupling is also very important. In the past years, different current injection mechanisms in the substrate have been examined[1, 2]. Recently, lumped models for heavily and lightly doped substrates were proposed[3,4], and numerical techniques for efficient calculation of substrate resistance in macro-model were investigated [5]. Research on the minimization of substrate noise in the mixed-signal ICs is still undergoing. The use of guard ring, trench isolation, and SOI process, however, is believed to reduce the impact of substrate noise [6, 7].

## 1 Circuit Analysis

In this work, a few benchmark circuits in the mixed-signal circuit simulation are evaluated. The digital circuit portion is modeled through a large CMOS inverter. The input pulse of the inverter is designed to reflect the operation frequency of the current technology, in which the high operation frequency is about 2.5 GHz and the rise/fall time of the pulse is 0.5 ns and 0.5 ns respectively. For the analog circuit portion, the current source and current mirror are considered.

Fig. 1 shows the simplified layout of CMOS logic injection into the n-channel transistor in the current source [8]. The substrate is excited by CMOS inverters through the depletion/coupling capacitor. A single-transistor NMOS current source is used to measure the noise in the substrate. Substrate voltage fluctuations affect the current flowing in the current source via thresholds voltage variations (body effect) and capacitive coupling between the substrate and the gate, drain, source node. The substrate is biased using $p^+$

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substrate contact diffusions that are connected to bonding pads. The heavily doped (general doping density is above $10^{18}$ $cm^{-3}$) substrate is adopted because in the modern CMOS ICs this is usually the case to prevent the CMOS latch up.

In the equivalent circuit, the substrate is modeled as a single node due to its high substrate conductivity, hence the current spikes injected into the substrate will distribute on the substrate uniformly. We investigate this conclusion with below simulation using device simulator SILVACO.

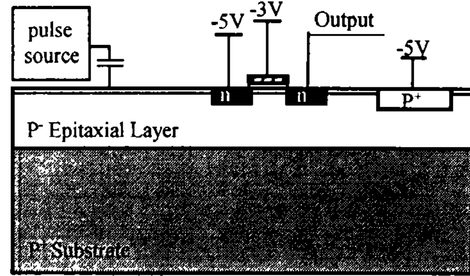


Fig. 1　Basic layout of the circuit with current source

For the simulation purpose, we construct the substrate structure by a heavily doped $p^+$ material (doping concentration is about $10^{19}$ $cm^{-3}$) and over the heavily doped substrate we apply a single layer of thin epitaxial layer of lightly doped $p^-$ material (doping concentration is $10^{15}$ $cm^{-3}$). The dimensions of the substrate are, we consider here, the length 400 μm, the width 50 μm, the depth of the substrate 80 μm and the thickness of the epitaxial layer 20 μm. The simplified test structure is shown in Fig. 2. The pulse generator has the width of 8 ns, of which the rise/fall time is 1 ns respectively and the width 6 ns. The delay time of 6 ns is also used. Fig. 3 shows the simulation result of the current vectors.

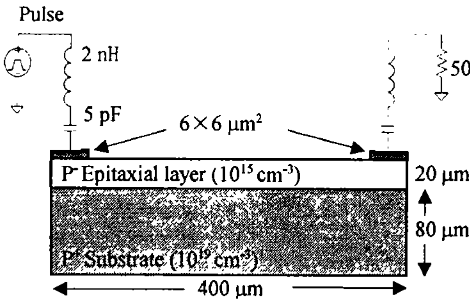


Fig. 2　SILVACO simulation structure

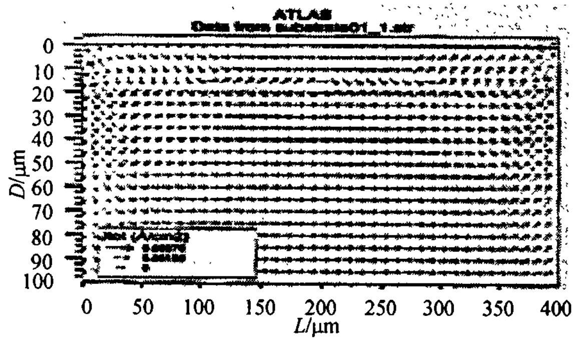


Fig. 3　Current flow distribution for heavily doped substrate with exitaxial layer

From the simulation result it is seen that the current flows vertically down from the first contact to the heavily doped substrate. Then the current flows uniformly through the heavily doped substrate to the second contact. This shows that the resistance of the heavily doped substrate is much less than the resistance of the lightly doped epitaxial layer. The uniform current flow in the substrate indicates that the resistance of the heavily doped substrate is so small that it can be considered as a single node (Bulk node).

For different substrate systems such as multi-layer substrate and SOI structure, the substrate model is more complicated and the model should consist of distributed resistance and capacitance. The equivalent mixed-signal circuit for the examination of the substrate noise coupling is shown in Fig. 4. In Fig. 4, $L_s$ and $R_s$ represent the wire impedance from the package and $C_s$ represents the on-chip parasitic capacitance. Since the values of components $L_s$, $R_s$, and $C_s$ are all highly dependent on the IC package (or actual physical devices), they are taken directly from the values used by Su[8],rather than be actually calculated. A schematic representation of the current mirror for SPICE circuit simulation is also shown in Fig. 5.

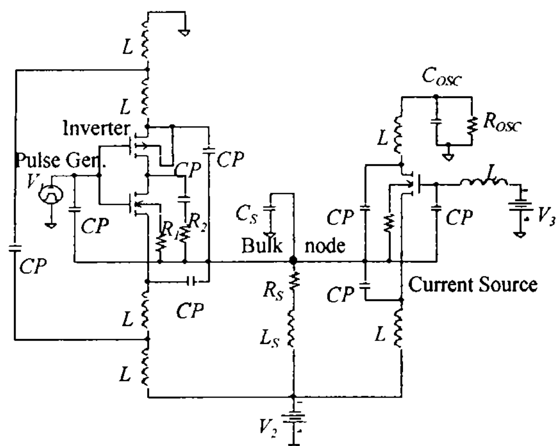


Fig. 4 Schematic representation of the circuit with current source for circuit simulation

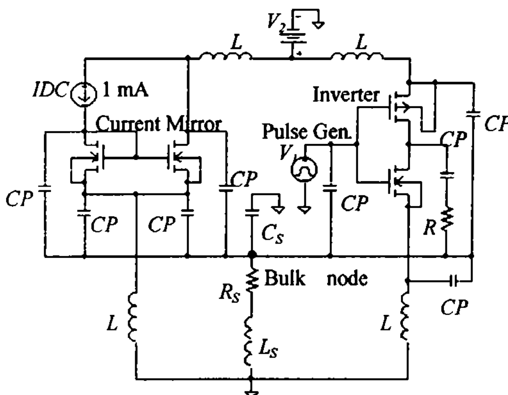


Fig. 5 Schematic representation of the circuit with current mirror for circuit simulation

## 2 Simulation Environment

The simulation environment used was OrCAD Pspice 8.0 for Microsoft Windows. This package allows full analog/digital simulations of almost any conventional circuit. The package consists of many sub-programs which provide a multitude of simulation and analytical tools. The programs used by the authors are Schematic Editor, PSPICE circuit simulation program, Probe program, and Stimulus Editor.

The operation of the transistors is complex due to their active nature. There exist a multitude of transistor models with varying degrees of accuracy. These models are made up of a set of equations and parameters. To get the simulation done and to be relatively simple, the level 1 model of CMOS device was chosen.

## 3 Results and Discussion

The equivalent circuit in Fig. 4 and Fig. 5 are simulated. The simulated noise waveform of the circuit in Fig. 4 is shown in Fig. 6. In this transient waveform, it is clear that the larger the package inductance is, the larger the noise voltage spike will be in the substrate. Fig.7 displays the noise current as a function of time for the mixed-signal circuit in Fig.5. The injection of the substrate produces a noise current oscillation around the desired output at 1.0 mA. The noise current spike is as high as 2.0 mA which is twice of the desirable output current.

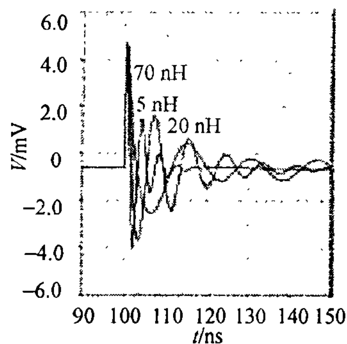


Fig. 6 Simulated noise waveform of the circuit of Fig. 4

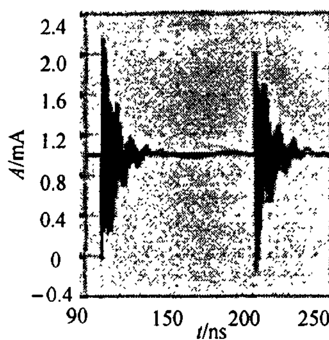


Fig. 7 Simulated noise waveform of the circuit of Fig. 5

The SPICE simulation results of the above two simplified mixed-signal circuits highlight the significance of the substrate noise coupling in the mixed-signal IC design. More circuit design issues should be studied.

# 4 Conclusion

The methodology to analyze the mixed-signal circuits has been demonstrated. Modeling of the substrate of the mixed-mode IC in SPICE simulation has been developed. The sensitivity of device technology on the substrate noise coupling is examined.

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# 混合信号集成电路中的衬底噪声耦合*

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【摘要】 研究混合信号集成电路中衬底噪声耦合及衬底噪声对模拟/数字电路的影响。采用带外延层的重掺杂型衬底，对混合信号集成电路中研究衬底噪声的两个基准(Benchmark)电路进行了模拟和评价，提出了在高速和高频工作时应用 SPICE 对混和信号电路进行模拟的正确方法.

关 键 词 衬底噪声； 耦合； 混合信号集成电路； 模型

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