Design and Fabrication of a Low-Noise CMOS Charge Sensitive Amplifier*

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Abstract A new design of low-noise low-power consumption charge sensitive amplifier is presented. Simulated by EDA software Cadence, the results obtained are satisfied. The DC open-loop gain is 82.9 dB with a 28 kHz –3 dB bandwidth and its phase margin is 46.9°. The maximum output noise spectral density is 1.5 μV/Hz^2 at very low frequency. Using standard 3μm P-Well CMOS technology, the proposed amplifier is fabricated, and the measurement results are closed to the simulation.

Key words low-noise; charge amplifier; low power design; low voltage

低噪声CMOS电荷敏放大器设计与研制*

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【摘要】提出了一种新的低噪声低功耗电荷敏感放大器设计方案。用EDA软件Cadence进行模拟，得到了满意的仿真结果：直流开环增益为82.9 dB，f_{-3dB}为28 kHz，相位裕度为46.9°，低频下输出噪声频谱密度为1.5 μV/Hz^2。采用标准的3 μm P阱CMOS工艺进行了流片，测试结果与模拟情况相近。

关 键 词 低噪声; 电荷放大器; 低功耗设计; 低电压

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In order to achieve high rate high precision test for applications in particle physics, nuclear physics, and *X-b* imaging, charge sensitive amplifiers are widely used to sense the charges collected by the detector and to convert the charge signal to voltage signal. However, low-voltage supply and low-power consumption have emerged as a major theme today in amplifier design, especially when the amplifiers are used in the portable mini-type instruments. The noise performance of the charge amplifier has to be optimized.

As is well known, the Junction-FETs has a much better noise performance comparing to the Bipolar Junction Transistors and MOSFETs, but the process uniformity can't be well controlled, so it is not fit to realize very large scale integration[1]. The recent researches are focused on full CMOS circuits design[2~4].

The most important characteristic of the charge amplifier is low noise performance, which depends on the input transistor mostly. So the noise performance of input transistor and its bias current are very important. Normally, the noise performance of input transistor is mainly characterized by an equivalent input noise voltage source v_e[5]：

$$S_{v_e}(f)=\frac{8}{3}\frac{kT}{g_m}+\frac{K_f}{C^2{}_{ox}WL}\frac{1}{f} \tag{1}$$

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where g_m is the transconductance of input transistor. From (1), an important fact is that the channel thermal noise dominates the total noise contribution if the amplifier works at high frequency.

In order to reduce the thermal noise, the transconductance of the input transistor g_m must be increased. From the transconductance given in (2).

$$g_m = \sqrt{2mC_{ox}\frac{W}{L}I_{ds}} \tag{2}$$

the minimal channel length L is limited by the complementary metal-oxide-semiconductor (CMOS) process used. The increase of the channel width W impairs the high-frequency performance due to the increase of the input capacitance. One efficient possibility is the increase of the bias current I_{ds}. As a result, a high-power consumption cannot be avoided in the amplifier. So there must be a tradeoff between the noise and the power consumption. In this paper, we describe a new design and fabrication of a low-noise and low-power consumption charge amplifier, some of the simulation and measurement results are presented.

1 Charge Amplifier Topology and Analysis

The proposed low-noise low-power consumption amplifier topology is shown in Fig.1. Utilizing low-voltage technology, the circuit is single voltage supplied, and the V_{dd} is only 3 V, which reduces the whole power consumption.

The transistors M_1, M_2, M_3, and M_4 construct the first stage, in which M_1 and M_3 consist of a cascode amplifier with high-gain high-output impedance. The transistors M_5 and M_6 consist of a source follower, which gives two advantages. First, the transistor M_5 adjusts the output potential in order to bias the input transistor correctly. Second, a lower output impedance is obtained which can efficiently drive the next readout system.

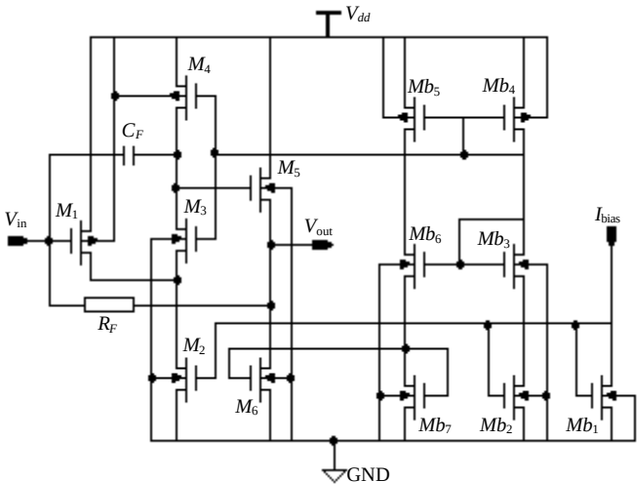

Fig.1　Topology of the charge amplifier

The other transistors in this circuit, Mb_1~Mb_7 consist of a bias block to supply the needed bias voltages for the amplifier stage and source follower.

According to the small-signal equivalent circuit of the amplifier without feedback resistor and capacitor, the DC open-loop gain A_v can be calculated as

$$A_v \approx -\frac{g_{m1}}{g_{ds4}} \tag{3}$$

and the dominant-pole of the open-loop amplifier is

$$P_1 \approx \frac{g_{ds4}}{C_{D4}} \tag{4}$$

where C_{D4} is the total capacitor at the transistor M_4.

2 Simulation Results

In order to investigate the feasibility of the proposed charge amplifier discussed above, a simulation has been performed with EDA software CADENCE using the SPICE model. The input transistor dimension is designed to be 6 000 μm/3 μm to obtain the tradeoff between noise and power consumption performances. A bias current 1 mA is taken for M_1.

The simulation results are presented in Table 1 and in Fig.2 and 3. It is observed that the DC open-loop gain and the bandwidth are suitable for the charge amplifying application, and the power consumption is low enough to the battery supply system.

The maximum output noise spectral density voltage is 1.5 μV/Hz^2 at very low frequency, which is small enough for the mostly charge signal amplifying and processing applications using capacitive detector.

Table 1 Cadence simulation results of the amplifier

Parameters	Performance
Power Supply/V	3
Open-loop Gain/dB	82.9
Open-loop Dominant-Pole/kHz	28.07
Unit-Gain Bandwidth/MHz	300
Power consumption/mW	4.5

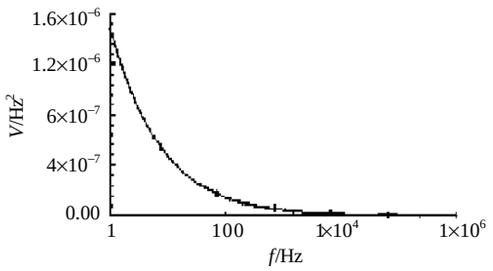

Fig.2 The curve of output noise spectral density

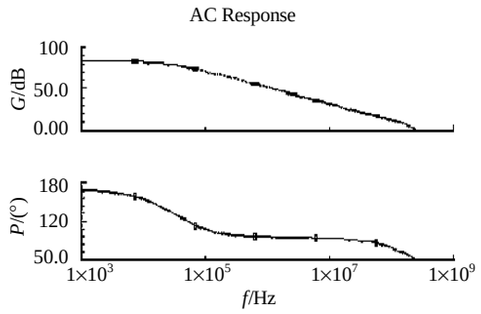

Fig.3 AC response of the amplifier

From Fig.3, we can obtain the phase margin at 46.9°, which will insure the stability of the amplifier in its working frequency range from 10～100 kHz.

Further more, the layout is also drawn as Fig.4 under the design rules of the foundry.

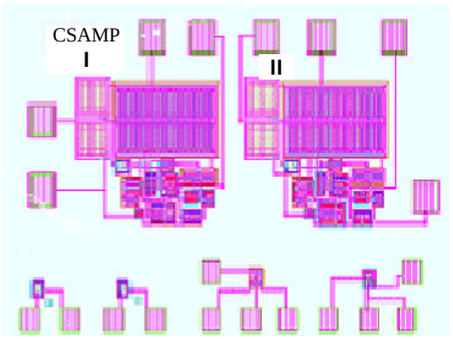

Fig.4 The layout of the circuit

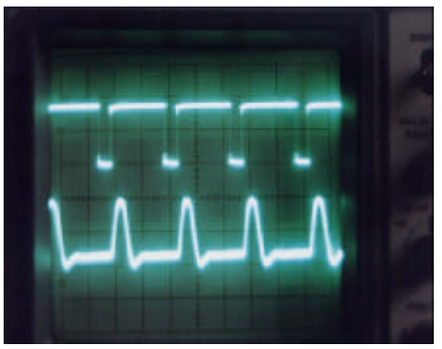

Fig.5 Measured transient characteristics

3 Fabrication and Measurement

The full CMOS charge sensitive amplifier proposed and designed above has been fabricated in poly-Silicon gate and P-Well CMOS technology, which critical dimension is 3 μm. The chips are packaged in 8-Pin DIP format. Using Oscillograph AROE BS601A, Pulse generator TFG-8111 and digital multimeter HP34401A, the monolithic amplifier is tested. When supply voltage from 2.6～4 V, this amplifier works quite well. Under 3 V supply voltage, the total bias current is 1.3 mA, and the power consumption about 5 mW, which is very similar to the simulation result. The equivalent input noise voltage is only 0.075 μV at 100 kHz frequency. The photographed transient characteristic is shown in Fig.5. The upper curve is 30 mV input signal, the lower one 60 mV output and their frequency 30 kHz.

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束自己的生命周期；

4) 若Agent迁移失败，仍由原代理负责接收消息。

因此在Agent的整个生命周期中，始终有且仅有一个代理负责接收发送给该Agent的消息，因而不会出现通信失效的情况。

5 结 束 语

为了促进MAS的开发、推动Agent间的协作计算以及相关问题的解决，本文就移动Agent在MAS环境下实现交互协作的几个关键问题做了一些探讨。目前，多Agent交互协作技术还不成熟，有许多问题有待深入研究，包括系统的结构和管理、设计任务的规划和分解、设计知识的表示和转换、主体的通信策略和语言、冲突的识别和消解、系统的安全性等。随着对多Agent系统理论与应用研究的不断深入，多 Agent技术也将日益得到完善，它将成为未来网络环境的主流技术。

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4 Conclusions

In this paper, we have presented a new design of low-noise low-power consumption charge amplifier. Simulated by EDA software Cadence, the results obtained are satisfied. The DC open-loop gain is 82.9 dB with a 28 kHz –3 dB bandwidth and its phase margin is 46.9°. And the maximum output noise spectral density is 1.5 $\mu V/Hz^2$ at very low frequency. Using standard 3 μm P-Well CMOS technology, the proposed amplifier is fabricated, and the measurement results are closed to the simulation. Due to its good performance, this kind of charge amplifier can be widely used in particle physics, nuclear physics, and γ-ray detection.

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